REMARKS/ARGUMENTS

Claims 1-30 were previously pending in the application. Claim 27 is canceled; claims 6, 16, 21 and 28 are amended; and new claims 31-33 is added herein. Assuming the entry of this amendment, claims 1-26 and 28-33 are now pending in the application. The Applicant hereby requests further examination and reconsideration of the application in view of the foregoing amendments and these remarks.

In paragraph 2 of the office action, the Examiner rejected claims 1, 3-11, and 13-30 under 35 U.S.C. 102(e) as being anticipated by Li. In paragraph 16, the Examiner objected to claims 2 and 12 as being dependent upon a rejected base claim, but indicated that those claims would be allowable if rewritten in independent form. For the following reasons, the Applicant submits that all of the now-pending claims are allowable over Li.

Claims 1 and 11

Claim 1 is directed to a scheduler for a plurality of packet storage devices. The scheduler comprises a memory device, a latch, and an extractor. The memory device stores a look-up table (LUT) that maps an input address to a LUT output, where (1) the input address corresponds to the current status of one or more of the packet storage devices and (2) the LUT output identifies the next packet storage device to select for service and whether the next packet storage device has data available for service. The latch stores and forwards the LUT output. The extractor receives the forwarded LUT output from the latch and generates (1) a latch enable (LE) control signal that enables the latch to forward the LUT output and (2) a read enable (RE) control signal that identifies which one or more packet storage devices are to be serviced.

Fig. 1 shows an exemplary embodiment (100) of the scheduler of claim 1, where:

- FIFO_0 and FIFO_1 of Fig. 1 are examples of the plurality of packet storage devices of claim 1;
- ROM 102 of Fig. 1 is an example of the memory device of claim 1;
- Bits S0, S1, and Cp of Fig. 1 form an example of the input address of claim 1;
- Bits Np and $SERV_N$ of Fig. 1 form an example of the LUT output of claim 1, where bit Np identifies the next packet storage device to select for service and $SERV_N$ identifies whether the next packet storage device has data available for service;
- Latch 104 of Fig. 1 is an example of the latch of claim 1; and
- Extractor 106 of Fig. 1 is an example of the extractor of claim 1, where extractor 106 receives the forwarded LUT output Q0, Q1 from latch 104 and generates (1) latch enable control signal LE, which enables latch 104 to forward the LUT output D0, D1 as the forwarded LUT output Q0, Q1 and (2) read enable control signal RE[1:0], which identifies which one or more packet storage devices are to be serviced.

For the following reasons, the Applicant submits that Li does not teach or even suggest the invention of claim 1.

Li teaches a weighted round-robin arbitrator for servicing a number of queues. For example, Fig. 2 shows a system for servicing three queues. In particular, Fig. 2 shows a slot entry table 202 having a number of slots 204-218. As described in paragraphs [0014]-[0015], slot entry table 202 (i) receives three empty flags 224, each of which indicates whether or not the corresponding queue is empty and (ii) generates queue select signal 222, which identifies which of the three queues is to be serviced. In addition, slot entry table 202 feeds table entry TE of slot 204 back to be the new table entry for slot 218, as part of a process of shifting all of the table entries one slot to the left.

Note that queue select signal 222 can be but does not have to be equal to table entry TE of slot 204. In particular, queue select signal 222 will be equal to table entry TE of slot 204 only when the queue associated with slot 204 is not empty. If the queue associated with slot 204 is empty, then queue select signal 222 will not be equal to table entry TE of slot 204. See paragraph [0015].

Li's Fig. 3 shows a detailed implementation of two contiguous slots of slot entry table 202 of Fig. 2, where TE output 310 of Fig. 3 is analogous to TE 220 of Fig. 2, and signal 314 of Fig. 3 is analogous to queue select signal 222 of Fig. 2. See paragraph [0016]. Thus, circuits 302 and 352 of Fig. 3 may be said to correspond to slots 204 and 206, respectively, of Fig. 2. As shown in Fig. 3, slot 302 includes table entry 308, which contains the address of the queue to be selected when slot 302 is active. See paragraph [0017]. Each slot also includes two muxes 312 and 316, which determine whether signal 314 identifies the queue address 310 stored in table entry 308 or the daisy-chained queue address 364 from previous slot 352. As indicated earlier, if the queue associated with slot 302 is empty, then muxes 312 and 316 operate to select the daisy-chained queue address 364 to be output on signal 314.

Given this understand of the teachings in Li, it is clear that Fig. 3 shows more-detailed block diagrams of two of the slots of slot entry table 202 shown in Fig. 2. Fig. 3 does not teach circuitry that is distinct or otherwise different from the circuitry of slot entry table 202 shown in Fig. 2.

In rejecting claim 1, the Examiner stated that Fig. 2 shows an example of the scheduler of claim 1, where (i) slot entry table 202 is an example of the memory device of claim 1, (ii) empty flags 224 form an example of the input address of claim 1, and (iii) signal 310 or signal 314 of Fig. 3 is an example of the LUT output of claim 1. In addition, the Examiner indicated that table entries 308 and 358 are examples of the latch of claim 1, that signal 306 is an example of the latch enable (LE) control signal of claim 1,and that signal 315 or, in the alternative, signal 314 is an example of the read enable (RE) control signal of claim 1. The Applicant submits that the Examiner mischaracterized the teachings in Li in rejecting claim 1.

First of all, the Applicant submits that the Examiner improperly characterized slot entry table 202 and circuitry within slot entry table 202 as being distinct elements. In particular, claim 1 recites a scheduler comprising a memory device, a latch, and an extractor. In rejecting claim 1, the Examiner cites slot entry table 202 as being an example of the memory device of claim 1, while citing table entries 308 and 358 as being examples of the latch of claim 1. But table entries 308 and 358 are circuit elements of a detailed implementation of slot entry table 202; they are not distinct elements.

The Examiner cannot have it both ways. If slot entry table 202 is an example of the memory device of claim 1, then table entries 308 and 358 are part of that memory device, in which case, Li does not teach a latch that is distinct from slot entry table 202. If, on the other hand, table entries 308 and 358 are latches that are distinct from Li's storage device, then it is not clear what elements taught in Li constitute a storage device, because table entries 308 and 358 are the only elements taught in Li that store data that can in any way be said to correspond to a look-up table.

Significantly, in rejecting claim 1, the Examiner does not even cite any hardware taught in Li as corresponding to the extractor of claim 1. According to claim 1, the extractor receives the forwarded LUT output from the latch and generates (1) a latch enable (LE) control signal that enables the latch to forward the LUT output and (2) a read enable (RE) control signal that identifies which one or more packet storage devices are to be serviced.

Li teaches only two signals that can possibly be considered to be a LUT output: output signal 314 and feedback signal 310. Li teaches that output signal 314 is applied to a queue multiplexer (not shown in Fig. 3) to select the appropriate queue for data to be sent out. See paragraph [0018]. There is absolutely no teaching in Li that output signal 314 is applied to anything resembling the extractor of claim 1.

Li also teaches that feedback signal 310 is applied (i) to the table entry of the next slot and (ii) to a mux in the next slot. Since the Examiner has already indicated that he believes that Li's table entries are examples of the latch of claim 1, presumably the Examiner does not also believe that Li's table entries are examples of the extractor of claim 1. That leaves only muxes like muxes 312 and 362 as being part of Li's extractor. According to claim 1, the extractor generates a latch enable (LE) control signal that enables the latch to forward the LUT output. There is no teaching anywhere in Li that Li's muxes 312 and 362 are part of any circuitry that generates such a latch enable (LE) control signal.

The Examiner suggests that signal 306 is an example of the latch enable (LE) control signal of claim 1. But Li clearly identifies signal 306 as being a clock signal. See paragraph [0017]. Even if Li's table entry 308 were considered to be an example of the latch of claim 1 (which the Applicant does not admit), Li's clock signal 306 is simply not a latch enable signal, as that term is understood by those skilled in the art. Nor does Li identify or describe the source of either clock signal 306 or POP signal 304.

The Examiner also suggests that signal 315 or, in the alternative, signal 314 is an example of the read enable (RE) control signal of claim 1. Since claim 1 recites that the extractor generates the read enable (RE) control signal, to be consistent, the Examiner's suggestion implies that muxes 312 and/or 316 would be part of Li's extractor. As suggested previously, there is no suggestion in Li that muxes 312 and/or 316 have anything to do with generation of a latch enable (LE) control signal.

Furthermore, according to claim 1, the LUT output identifies a next packet storage device to select for service and whether the next packet storage device has data available for service. While it is true that Li's signal 314 identifies the next packet storage device to select for service, signal 314 does not identify whether the next packet storage device has data available for service. In particular, Li does not address the case when all queues are empty. It is not even clear what value Li's slot entry table 202 will output if all of the queues are empty. In the invention of claim 1, on the other hand, the LUT output identifies both (1) the next packet storage device to select for service and (2) whether that selected packet storage device has data available for service. Li's signal 314 identifies the former, but not the latter.

Since Li does not teach all of the elements of claim 1, Li does not meet the requirements of an anticipatory reference. Nor does the prior art suggest the elements of claim 1 that are missing from Li.

For all these reasons, the Applicant submits that claim 1 is allowable over Li. For similar reasons, the Applicant submits that claim 11 is allowable over Li. Since claims 2-10, 12-20, and 31-32 depend variously from claims 1 and 11, it is further submitted that those claims are also allowable over Li.

Claims 3 and 13

According to claim 3, the extractor comprises an FSM having an IDLE state and an EXTRACT state. When the FSM is in the IDLE state and a currently selected packet storage device has no data available for service, the extractor sets the LE control signal to enable the latch to forward the LUT output. When the FSM is in the EXTRACT state and service of the currently selected packet storage device is completed, the extractor sets the LE control signal to enable the latch to forward the LUT output.

As mentioned in the previous section, the Examiner did not explicitly identify any hardware in Li as corresponding to the extractor of claim 1. Nevertheless, in rejecting claim 3, the Examiner stated that "the extractor can be said to be in EXTRACT state when it is extracting data from the selected queue and is in IDLE state when it is not extracting." Yet, Li contains no teaching of a finite state machine, let alone an FSM having an IDLE state and an EXTRACT state.

If Li's extractor can be said to be in EXTRACT state when "it" is extracting data from the selected queue, then perhaps Li's extractor is the queue multiplexer mentioned in paragraph [0018]. But there is no teaching in Li that that queue multiplexer sets the LE control signal. Moreover, according to the Examiner, clock signal 306 is an example of the LE control signal of claim 3. In that case, Li's queue multiplexer would somehow generate Li's clock signal 306. But Lit contains no such teaching.

The Applicant submits that this provides additional reasons for the allowability of claim 3 and similarly for claim 13 (and for claims 4 and 14 which depend from claims 3 and 13) over Li.

Claims 5 and 15

According to claim 5, the current status of the one or more packet storage devices comprises an indication of whether each packet storage device has data available for service and an indication of which packet storage device is currently selected for service. Since, according to claim 1, the input address corresponds to the current status, claim 5 implies that the input address corresponds to both (1) an indication of whether each packet storage device has data available for service and (2) an indication of which packet storage device is currently selected for service.

While Li's input address (e.g., empty flags 224 of Fig. 2) may be said to indicate whether each of Li's queues has data available for service, there is no teaching in Li that Li's input address corresponds to an indication of which packet storage device is currently selected for service. In rejecting claims 5 and 15, the Examiner cited empty flags 224 of Fig. 2 and empty flags 318-322 of Fig. 3. None of these flags indicates in any way which packet storage device is currently selected for service.

The Applicant submits that this provides additional reasons for the allowability of claim 5 and similarly for claim 15 (and for claims 6 and 16 which depend from claims 5 and 15) over Li.

Claims 6 and 16

Claims 6 and 16 have been amended to further distinguish over Li. In particular, according to currently amended claims 6 and 16, a packet storage device has data available for service when the packet storage device currently stores more than a specified non-zero threshold number of data packets. Support for the amendments to claims 6 and 16 are found on page 3, lines 15-17, of the specification.

As the Examiner states in paragraph 7, Li teaches only that "the packet storage device has data available when it is not empty, i.e., more than zero." This corresponds to a threshold number of data packets of zero. Using a non-zero threshold number of data packets, as recited in currently amended claims 6 and 16, implies that a packet storage device could have one or more data packets and still not yet be "available for service." Li does not teach or even suggest such a feature. The Applicant submits that this provides additional reasons for the allowability of claims 6 and 16 over Li.

Claims 7 and 17

According to claim 7, the extractor is further adapted to receive service status information from the packet storage devices. In Fig. 1 of the present application, EOP[1:0] is an example of the service status information of claim 7.

In rejecting claim 7, the Examiner stated that "Li discloses, in page 2 paragraph 15, that once data has been sent out, the table is rotated. This requires indication of completion of service." Here, too, the Examiner's argument breaks down over the failure to identify what elements in Li correspond to the extractor of the claimed invention.

According to claim 17, the LE and RE control signals are generated based on service status information from the packet storage devices. The Examiner does not indicate how service status information from Li's packet storage devices is used to generate Li's clock signal, which the Examiner stated was an example of the LE control signal of the claimed invention.

The Applicant submits that this provides additional reasons for the allowability of claim 7 and for claim 17 (and for claims 8 and 18 which depend from claims 7 and 17) over Li.

Claim 21

Claim 21 has been amended to recite the features of original claim 27. As such, currently amended claim 21 is directed to a scheduler for a plurality of packet storage devices, wherein the scheduler comprises a look-up table (LUT) that identifies a next packet storage device to select for service based on current status of one or more of the packet storage devices, where the current status of the one or more packet storage devices comprises an indication of whether each packet storage device has data available for service and an indication of which packet storage device is currently selected for service.

For the same reasons provided earlier for claims 5 and 15, the Applicant submits that currently amended claim 21 is allowable over Li. Since claims 22-26, 28-30, and 33 depend variously from claim 21, the Applicant submits that those claims are also allowable over Li.

Claim 22

According to claim 22, the scheduler further comprises (1) a latch adapted to store and forward the identification of the next packet storage device to select for service based on a latch enable (LE) control signal and (2) a finite state machine (FSM) adapted to (1) forward the identification of the next packet storage device to the plurality of packet storage devices and (2) generate the LE control signal, based on service status information from the packet storage devices. For at least some of the same reasons provided earlier for claims 1 and 11 and claims 3 and 13, the Applicant submits that this provides additional reasons for the allowability of claim 22 (and therefore claims 23-26) over Li.

Claim 23

For at least some of the same reasons provided earlier for claims 3 and 13, the Applicant submits that this provides further reasons for the allowability of claim 23 (and therefore claims 23-26) over Li.

Claim 25

For at least some of the same reasons provided earlier for claims 8 and 18, the Applicant submits that this provides further reasons for the allowability of claim 25 (and therefore claim 26) over Li.

Claim 28

For at least some of the same reasons provided earlier for currently amended claims 6 and 16, the Applicant submits that this provides further reasons for the allowability of currently amended claim 28 over Li.

New Claims 31-33

According to new claims 31 and 32, the read enable (RE) control signal is adapted to simultaneously identify that two or more packet storage devices are to be serviced. According to new claim 33, the scheduler is adapted to simultaneously identify that two or more packet storage devices are to be serviced. Support for new claims 31-33 is found on page 7, line 33, to page 8, line 2, of the specification.

In Li, one and only one queue is "simultaneously" identified for service by signal 314. As such, the Applicant submits that this provides additional reasons for the allowability of claims 31-33 over Li.

In view of the foregoing, the Applicant respectfully submits that the rejections of claims under Section 102(e) have been overcome.

In view of the above amendments and remarks, the Applicant believes that the now-pending claims are in condition for allowance. Therefore, the Applicant believes that the entire application is now in condition for allowance, and early and favorable action is respectfully solicited.

Respectfully submitted,

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